ECM44 Very Large Scale Integrated Circuits (VLSI)

866

REG. NO

OCTOBER 2021

Time: Three hours

Maximum Marks: 75

Note:
1. Answer ALL the questions in PART-A (1 mark each)
2. Answer any ONE question from each unit in PART-B (3 marks each)
3. Answer any ONE question from each unit in PART-C (10 marks each)
4. The question paper contains TWO Pages

PART-A (1x10=10)

1. Draw the symbol of NMOS.
2. What is SOP?
3. Expand VHDL.
4. Define the term simulation.
5. What is entity?
6. Write any two data types of VHDL.
7. Write the entity declaration of D flip flop.
8. Define state Diagram.
9. What is PLA?
10. Mention the applications of FPGA.

PART-B (3x5=15)

UNIT-I

11. Draw the diagram of CMOS as a NOT gate.
12. Write about CMOS transmission gates.

UNIT-II

13. Give short notes on process statement.
14. Write the VHDL code for OR gate.

UNIT-III

15. Give short notes on event scheduling.
16. Draw the design unit of package in VHDL.

UNIT-IV

17. Write a VHDL code for T flip flop with reset.
18. Write a VHDL code for 3 bit down counter.

UNIT-V

19. Differentiate between CPLD and FPGA.
20. What is PLD? List the types of PLD.

PART-C (10x5=50)

UNIT-I

21. Draw the internal circuit diagram of CMOS OR gate and explain its operation.
22. Implement the function $F=\Sigma m(0,2, 3, 7)$ with don't care of 4 and 6 with minimal gates and implement the function using multiplexer.

UNIT-II

23. Explain CAD tool and the tasks performed by each tool.
24. (A) Write the VHDL code for implementing 4:1 multiplexer.
    (B) Write the VHDL code for NOR gate.

UNIT-III

25. Explain sequential statement in detail.
26. Explain in detail about behavioral modeling.

UNIT-IV

27. Write a VHDL code for JK flip flop with and without reset input.
28. Explain Moore type serial adder in detail.

UNIT-V

29. Explain combinational logic design using PAL.
30. Draw CPLD architecture and explain in detail.

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